Volume 09 Issue 01 Published, February 17, 2005 ISSN 1535-864X DOI: 10.1535/itj.0901

Intel® Technology Journal

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Low-Power Audio and Storage Input/Output Technologies for the Second-Generation Intel® Centrino™ Mobile Technology Platform

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Low-Power Audio and Storage Input/Output Technologies for the Second-Generation Intel® Centrino™ Mobile Technology Platform

Tom Clark, Mobility Group, Intel Corporation
Feng (Frank) Yang, Mobility Group, Intel Corporation
Greg Kaine, Mobility Group, Intel Corporation
Brian Leete, Mobility Group, Intel Corporation
Sriram Ranganathan, Mobility Group, Intel Corporation

Index words: High Definition Audio, Serial ATA, SATA

ABSTRACT

One significant challenge in new platform design is how to add new and improved capabilities without increasing the power required to provide a particular function. This paper focuses on two key Input/Output (I/O) technologies provided by the chipset: integrated audio and the interface to the storage device (hard drive). First, we examine the architectural features of Intel® High Definition (HD) Audio and compare them to the previous integrated audio solution, in terms of power. Second, we examine the architectural benefits of Serial AT Attachment (SATA), and we describe the power-saving techniques that enable increasing functionality while maintaining power.

INTRODUCTION

A key requirement for the next-generation platform built on Intel® Centrino™ mobile technology is increasing the functionality provided by the platform in general, and the chipset in particular, while not using more power than that used by the previous-generation platforms. Intel chipsets provide many I/O interfaces on the Input/Output Controller Hub (ICH). This platform uses the sixth generation of the ICH, known as the ICH6-M. Two key interfaces provided by the ICH6-M are audio and storage. Both interfaces require increased functionality and throughput. Increased functionality usually comes at the cost of a larger design (increased gate count), which translates into higher leakage power and higher active power. Higher throughput implies faster activity and/or wider data paths, which also imply higher power.

Intel HD Audio improves audio quality with a higher bit rate and wider data words than the previous implementation. Other features improve the end-user experience by adding new functionality, such as support for array microphones, audio jack retasking, and multiple audio streams. Intel HD Audio mitigates the power impact of these improvements at a system level by enabling the processor to enter deeper power states and power-savings states more frequently, even while the audio interface is actively employed, such as during CD or DVD playback.

Serial AT Attachment (SATA) will eventually replace the previous storage interface, known as Parallel AT Attachment (PATA) as the interface of choice for hard drives. SATA provides an immediate increase in storage interface headroom by increasing the maximum theoretical bandwidth from 100 MBps to 150 MBps. This ensures that the rate at which the platform transfers data to and from the hard drive will be limited by hard drive mechanics, not by the electrical interface. SATA achieves this high transfer rate with a high-speed serial interface, which reduces component product cost and which can decrease platform manufacturing costs. To overcome the power demand of a high-speed serial interface, SATA uses power-reduction protocols on the host (chipset) as well as the device (hard drive).

HIGH DEFINITION AUDIO ARCHITECTURE

Audio Codec '97 (AC'97) was the first standard for integrated audio. AC'97 is capable of delivering up to 96 kHz/20-bit playback in stereo and 48 kHz/20-bit in multichannel playback modes. AC'97 first appeared in Intel chipsets starting in 1999. However, as consumers increasingly use PCs for their entertainment and communication needs, the demand for audio capability is much higher than AC'97 can deliver. Intel HD Audio is the next-generation integrated audio solution for PCs.

Intel HD Audio is expected to allow the integrated audio solution to keep pace with PC audio advances for the next ten years or more. The next-generation PC platform built on Intel Centrino mobile technology will be the first mobile platform with Intel HD Audio. It will gradually replace AC'97 over the next few years. Table 1 provides a summary of the key advantages of Intel HD Audio over AC'97.

Table 1: Feature comparison of AC'97 to Intel HD Audio

Feature	AC'97	Intel HD Audio
Streams	single stream (in and out)	up to 15 input and 15 output streams at one time and up to 16 channels per stream
Bandwidth	11.5 Mbps maximum	48 Mbps per SDO 24 Mbps per SDI
Bit Rate	up to 20-bit, 96 kHz	up to 32-bit, 192 kHz
DMA Usage	predefined	dynamic
Bandwidth Assignment	fixed	dynamic
Analog Plug-and-Play	limited	comprehensive
Power Management	none	idle detection, fine-grained power control
Microphone Array	2-elements	up to 16-elements
Driver SW	developed by audio codec supplier	OS native bus driver and Independent Hardware Vendor value-added function driver
Docking	none	enabled
HW Configuration	fixed	dynamic device enumeration

Intel HD Audio Hardware Architecture

In this section we provide a conceptual overview of Intel HD Audio. Our intention is not to provide any detailed or quantitative definition. For more information, refer to [6].

Intel HD Audio hardware architecture consists of three major components: a controller, a link, and a codec. The hardware building blocks of the architecture are shown in Figure 1.

Intel HD Audio Controller

The controller is connected to the system memory via a Peripheral Component Interconnect (PCI) Express*

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interface. It implements a memory mapped register interface for standard programming access. One or more Direct Memory Access (DMA) engines transfer audio "streams" between the system memory and codec(s) connected to the Intel HD Audio link. Each DMA engine in the controller can be set up to transfer a single "stream" between the system memory and one or more codecs.

Intel HD Audio Link

The audio link is a digitized serial interface that conveys data between the Intel HD Audio controller and the codecs. The controller is connected to one or more codecs via the audio link. Figure 2 shows how to connect an Intel HD Audio controller to codecs.

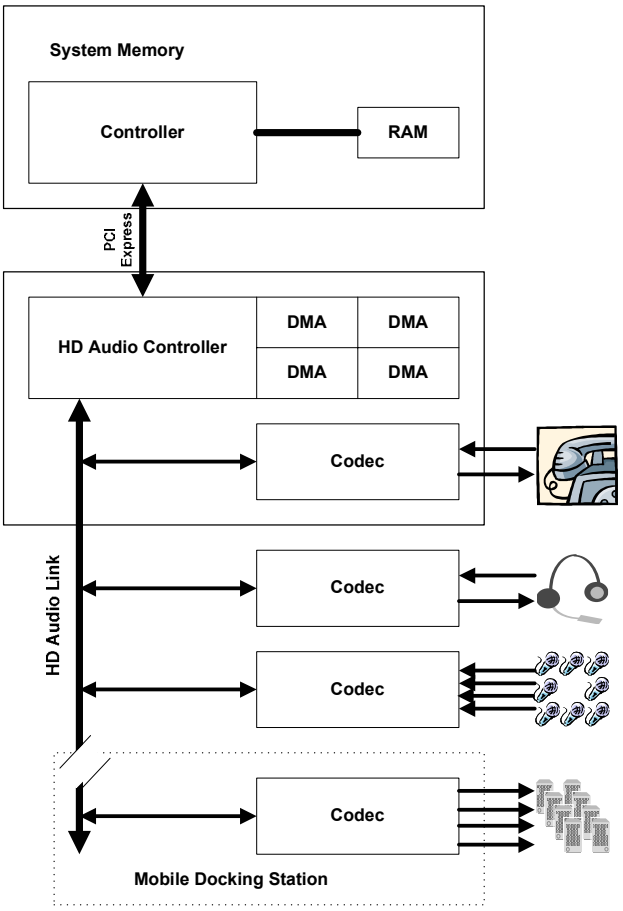

Figure 1: Intel HD Audio architecture block diagram

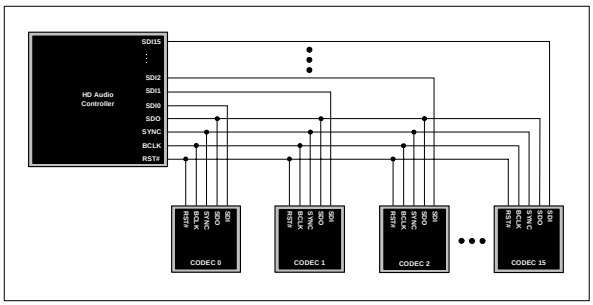

Figure 2: Example Intel HD Audio system

The link protocol is synchronized by the Intel HD Audio controller. It is purely isochronous with a 48 kHz framing period.

The Intel HD Audio link uses existing AC'97 signals with some changes:

- *Reset*. Also used to supply codec addresses.
- *Clock*. Rate is increased to and from the Intel HD Audio controller to codecs.
- *Sync to codecs*. Aligns frames and delineates outbound stream.
- *Serial Data Out (SDO).* Broadcast to all codecs.
- *Serial Data In (SDI).* Point to point, one or more per codec.

Figure 3 illustrates an example transaction on the Intel HD Audio interface.

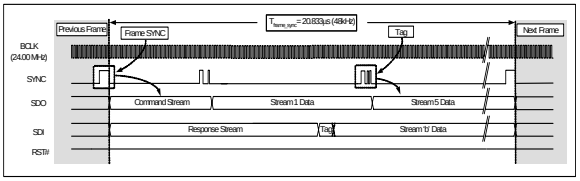

Figure 3: Intel HD Audio frame showing output command and data stream and input response stream

Codec

A codec is a physical device connected to the Intel HD Audio link. A single codec may contain one or more function groups.

- For output, it extracts one or more audio streams from an Intel HD Audio frame and converts them to an output stream through one or more converters.
- For input, it collects the data streams from one or more converters, frames them into Intel HD Audio frames, and sends them to the Intel HD Audio controller for processing.

Function Group
A function group is a collection of widgets that are all common to a single application/purpose and that are controlled by a single function driver. A widget is the smallest enumerable and addressable module within a function group. For each widget, there is a defined set of standard parameters and controls.

Intel HD Audio Software Architecture

Intel HD Audio software architecture is a layered architecture as shown in Figure 4.

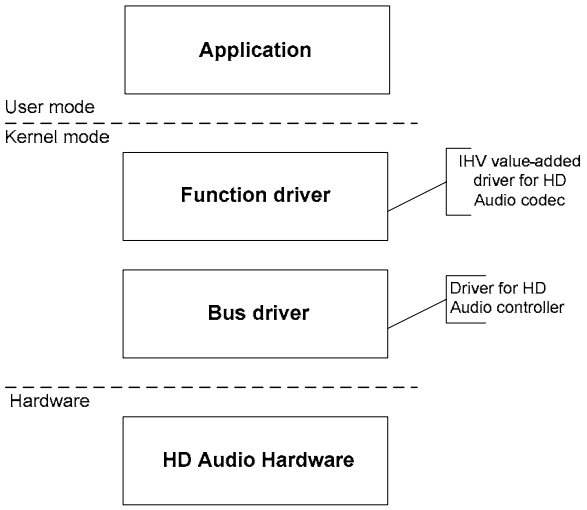

Figure 4: Intel HD Audio Software Driver Stack

Intel HD Audio Bus Driver
The Intel HD Audio Bus Driver has direct access to the HD controller register interface. It is responsible for the following:

- Initialization of the Intel HD Audio controller and link.
- Enumeration of all codecs on an Intel HD Audio link.
- Run-time management of Intel HD Audio controller and link, including power management.

Intel HD Audio defines a robust initialization model wherein the operating system can discover all of the codecs present and then can allocate system resources, such as memory, I/O space, and interrupts to create an optimal system environment. Intel HD Audio also defines a robust discovery mechanism for the codecs that are added at run time.

Intel HD Audio Function Driver
In most cases, the Intel HD Audio function driver is provided by codec vendors. It must implement a set of the standardized commands as defined in Intel HD Audio Specification 1.0. In general, it is responsible for the following:

- Initialization/reset of codec.
- Codec command processing.
- Management of codec topology and configuration.
- Management of streaming operation.

Intel HD Audio Power Management Architecture

Intel HD Audio provides building blocks for fine-grained power management. It defines power states for links and codecs. In most cases, all power-management controls are driven by software. Intel HD Audio also defines power widgets for power-management purposes. A power widget provides a single point of power state control for a predefined group of audio widgets. Power control to this widget effectively places all member widgets in the group in the prescribed power state. Fine-grained power management can be achieved with definitions of power widgets.

To enable more effective power management, the platform enables the CPU being put into sleep state while there is still an active stream on the Intel HD Audio link.

Intel HD Audio Docking Architecture

Intel HD Audio architecture is designed for docking support. It supports dynamic codec enumeration and defines a mechanism for heart beat detection in the link protocol. With appropriate chipset and software support, Intel HD Audio can be set up to have one or more Dolby 5.1/7.1 setups on a docking station.

Intel HD Audio Architecture for Digital Home and Digital Office

To meet emerging requirements for providing a surround sound experience with a variety of speaker configurations, Intel is working with Dolby Laboratories. Intel HD Audio can support all the Dolby technologies, including the latest Dolby Pro Logic IIx,* which makes it possible to enjoy older stereo content in 7.1 channel surround sound.

Intel HD Audio also supports the Sony/Philips Digital Interface (S/PDIF) that enables users to connect PCs to high end digital audio equipment.

Intel HD Audio not only provides an enriched playback experience, but it can also deliver a better quality input for voice and communication applications that are critical to a

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digital office usage model. Due to its new architecture and increased available bandwidth, Intel HD Audio can support up to a 16-element array microphone for higher quality input. One business application for array microphones is video conferencing, which could employ a voice-tracking camera, with noise cancellation over a Voice over Internet Protocol (VoIP) phone.

Jack retasking enables the host controller to redirect the audio stream to the correct device. In the case of a user plugging a headphone into a microphone jack, jack retasking will direct the headphone stream to the microphone jack.

Designed for Future

Intel HD Audio is a key building block of Microsoft's United Audio Architecture (UAA)*. UAA is a feature of the next Windows* Operating System (OS) codenamed "Longhorn." Intel HD Audio architecture is also extensible and can support any non-audio device connected to an Intel HD Audio link, as long as the device is compliant with the Intel HD Audio specification.

Intel HD Audio Architecture Summary

Intel HD Audio defines a new architecture that provides a significant performance increase compared to AC'97. It brings a consumer-electronics level of audio experience to PCs. Furthermore, it provides building blocks to enable emerging usage models for the PC as a family entertainment hub, i.e., a collaboration and communication device.

INTEL HIGH DEFINITION AUDIO POWER FEATURES AND RESULTS

Intel HD Audio System Power-Savings Design

The battery life of a mobile device is dependent upon platform power consumption. Intel HD Audio has been implemented with this understanding and enables techniques that can provide significant power savings under certain usage models. Intel HD Audio does this by allowing the CPU to enter a lower power ACPI idle state (C4) under certain conditions. In contrast, AC'97 will only allow the CPU to go as deep as C2, a state that consumes greater power than C4. Workloads that contain continuous audio streams such as CD audio playback and DVD playback can take advantage of this deeper power-saving state. Power savings are also achieved during idle periods with no audio playback. Intel HD Audio supports an efficient low-power ACPI idle state (D3) that it enters when no audio streams are being processed for an amount of time defined by the device driver.

When playing an audio stream using Intel HD Audio the CPU is allowed to enter C4, a low power CPU state. For AC'97 audio the depth of the CPU C-state is limited to C2 which consumes more power than C4. The ability of the CPU to enter this deeper sleep state with Intel HD Audio enables substantial power savings over AC'97. This power savings has been evaluated on an Intel reference board designed for taking power measurements.

Where the data stream resides is what permits this C-state behavior to occur. Intel HD Audio keeps data stream traffic in non-cached system memory and uses DMI VC1 to permit the Intel HD Audio controller to write or read these data without needing to snoop them on the processor. AC'97 keeps data stream traffic in cached system memory that must be snooped when the AC'97 controller writes or reads them. As a result the processor must always be in a snoopable C-state (C0-C2).

Intel HD Audio Power-Savings Results

CD audio playback and DVD movie playback are two common usage models that show the C4 power savings with Intel HD Audio as opposed to AC'97 audio. Both usage models generate isochronous data traffic thus allowing the benefits described above.

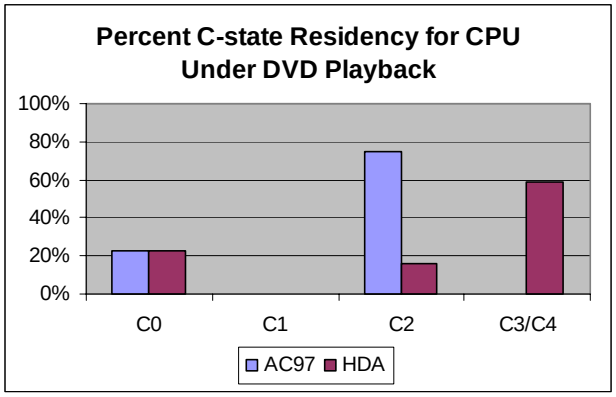

Figure 5: DVD playback CPU C-state residency

DVD playback shows a large shift in C2 residency to C4 as illustrated in Figure 5. C2 residency decreases from 75% with AC'97 audio to 16% for Intel HD Audio. This also results in an increase of C4 residency from 0% with AC'97 audio to 58% for Intel HD Audio. The shift in the distribution of C-states can result in a power savings of ~700 mW (see Figure 7). This power savings is almost entirely provided by the increased CPU residency in the lower power C4 state. Figure 5 also shows a significant CPU overhead in DVD decoding. Much of this overhead

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is due to video frames and not related to decoding audio. C1 residency is largely unaffected by either audio codec.

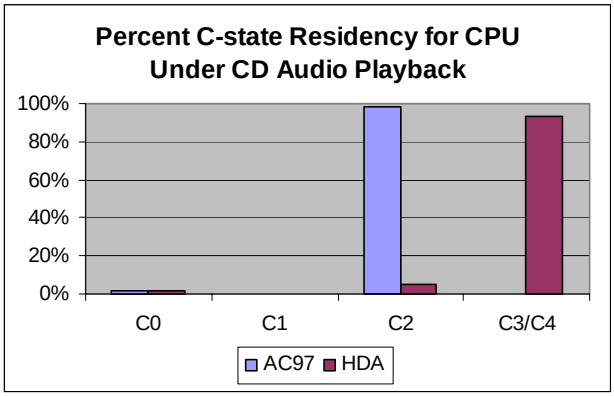

Figure 6: CD audio playback CPU C-state residency

CD audio (no video decoding overhead) shows an even greater shift in the CPU residency from C2 to C4. Figure 6 shows close to a complete shift of C2 residency to C4. C4 residency goes from 0% with AC'97 to 93% with Intel HD Audio, and there is a similar decrease in C2 residency from 98% (AC'97) to only 5% with Intel HD Audio. This large shift in CPU C-state residency results in power savings of ~850 mW as measured on the reference platform (see Figure 7).

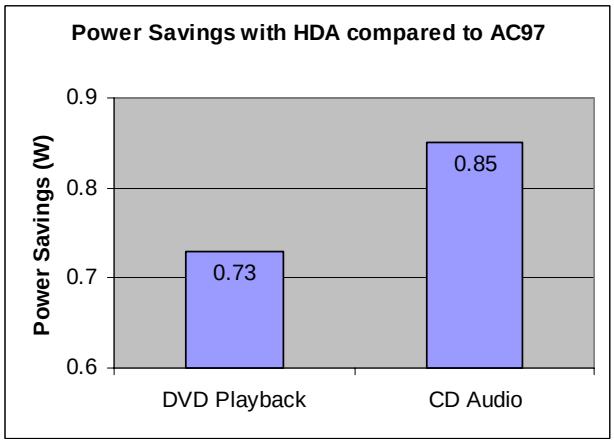

Figure 7: DVD and CD audio power savings

The impact on battery life of these power savings may be determined given the battery capacity and the average power for the given workload. For this analysis, platform average power for DVD playback is assumed to be in the range of 13 W to 17 W with Intel HD Audio. The percentage increase in battery life resulting from Intel HD Audio is directly related to the 700 mW decrease in power. Intel HD Audio could therefore potentially increase in battery life by as much as 8-17 minutes in DVD playback over a system configured with AC'97 audio.[1]

Similarly, for battery-life savings, analysis of CD audio playback power consumption in the range of 9 W to 13 W is assumed. The percentage increase in battery life resulting from Intel HD Audio is again dependent on the power savings of the workload. CD audio sees power savings of ~850 mW with Intel HD Audio. This power savings could potentially result in battery-life savings as much as 35-42 minutes in CD playback over a system configured with AC'97 audio.[1]

In addition to the power savings provided by Intel HD Audio during active workloads, there is also savings provided by the D3 low-power ACPI state when no audio stream is being processed. This low-power state brings Intel HD Audio power consumption down to levels on the order of tens of milliwatts. Without this feature, power consumption for the device could be as much as 10x greater when the device is idle. This can provide a ~5% decrease in power consumption for a platform at idle. A period of time is defined by the device driver that looks for any audio activity occurring during this period. If no activity is encountered the device is sent to the D3 state. A more power-friendly device driver would implement this period to be as small as possible in order to maximize power reduction. At the time of writing this paper the Windows driver for Intel HD Audio sets this value to a fairly aggressive period of five seconds.

SERIAL ATA ARCHITECTURE

Serial ATA (SATA) is the next generation of storage interface technology that is expected to replace Parallel ATA (PATA) in mobile systems. SATA provides many new features including: increased data transfer rates with increased protocol efficiency; low pin count interconnect with thinner flexible cables and connectors; decreased signaling voltage; enhanced error detection; and a point-to-point topology with the elimination of master/slave. It also includes support for Native Command Queuing, Native Hot Plug, Staggered Spin Up, and Port Multipliers. These new features are designed to provide both immediate value to the SATA subsystem today, and allow for future growth in storage technology over the next ten years. The following table compares SATA to PATA.

[1] Battery-life savings will vary with system configuration and platform power for a given workload. This range is based on battery capacities ranging from 54 Wh to 72 Wh with platform power for the workload at the minimum of the assumed range of power consumption.

Table 2: Feature comparison of SATA and PATA interfaces

Feature	PATA	SATA
Effective Data Rate	133 MB/Sec	150 MB/Sec 300 MB/Sec (Future) 600 MB/Sec (Future)
Connector Size	40	7
ICH6-M I/O Pins	27 (1 bus)	4 (per port)
Signaling Voltage	3.3 V	500 mV differential 250 mV common mode (nominal)
Error Detection	Data Only	Data and Commands
Point to Point Topology	No	Yes
Master/Slave Elimination	No	Yes
Native Command Queuing	No	Yes
Native Hot Plug	No	Yes
Staggered Spin Up	No	Yes
Port Multipliers	No	Yes
Link Power Management	N/A	Yes

In the ICH6-M, each SATA port consumes only 4 I/O pins (vs. 27 for PATA). Freeing up I/O pins allows additional functionality to be added to the chipset without increasing die size. Also, removing the requirement to provide the 3.3 V signaling that PATA requires, allows greater flexibility in adding future features to new chipsets.

On the motherboard, only four data traces to the drive need be provided to the drive for signaling purposes, and the SATA connector is correspondingly smaller, allowing more compact and efficient motherboard designs.

The SATA host controller in the ICH6-M can be configured to export one of two distinct software interfaces, a fully ATA backwards-compatible interface and a new SATA-specific Advanced Host Controller Interface (AHCI).

The AHCI specification supports the new SATA-specific features specified in SATA I and SATA II specifications. These include Native Command Queuing, Native Hot Plug, Staggered Spin Up, Port Multipliers, and Aggressive Link Power Management.

One of the basic challenges always present in introducing a new technology into the mobile platform is the additional power consumed by the added functionality. SATA Link Power Management can be used to limit the additional power consumption of the new SATA interface, providing the additional capability of SATA at the minimum power cost.

Link Power Management Overview

SATA Link Power Management puts the physical layer (PHY) of the link into a low-power state, independent of the ATA protocol power state of the disk, and as such complements the existing power management capabilities provided by the ATA command set. The ATA command set reduces the power consumption of the attached device by issuing protocol-level power state change requests to the disk. These requests typically instruct the device to spin down the media to save power.

Independent intelligent PHY power management has shown a significant reduction in the overall power consumption of the SATA subsystem, both in the platform and in the drive itself.

Link Power Management States

SATA provides two link power management states, in addition to the “active” state. These states are Partial and Slumber, that by specification, differ only by return latency. Partial has a maximum return latency of 10 microseconds, while Slumber has a maximum return latency of 10 milliseconds. Typical host and device hardware implementations should be able to realize greater power savings in Slumber with its longer specified return latency. Partial, therefore, is designed to allow link power state transitions continually with minimal impact on performance. Slumber is designed to be used only when the link is expected to be idle for an extended period of time. It is not possible to transition the link directly from Partial to Slumber without passing through the active state, as shown in Figure 8.

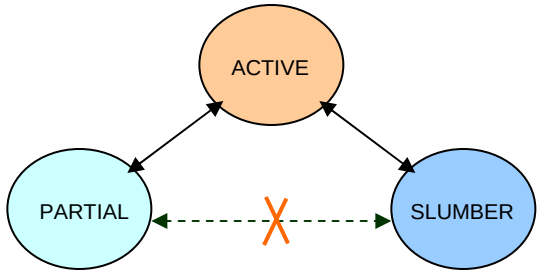

Figure 8: SATA power state transitions

Host- and Device-Initiated Power Management

SATA Link Power Management can be broken up into two basic types: Host Initiated Link Power Management (HIPM) and Device Initiated Link Power Management (DIPM).

SATA Link Power Management requires cooperation between the host and the device. Either the host or the device can request the link to enter a low-power state, but the corresponding host or device must accept or reject the link state change request. Each of these provides power savings by themselves; maximum power savings, however, are achieved when both are implemented together.

Host-initiated power management can be implemented either in the host hardware or the host software. In the first case, the host controller requests a link power management transition immediately after all outstanding commands to the drive have been completed. This allows the link to enter a low-power state immediately upon completion of the commands to the disk. Since the host has the best knowledge of what commands have been posted, or will be posted to the device, the host is able to make an immediate link power state change without invoking a time-out period.

Device-initiated power management is implemented by the drive. The drive knows best how long a specific command might take to complete, and is best equipped to request a link power management state change while processing the command.

The host controller on the host can automatically put the link into either Slumber or Partial after the command completes. Typically, for performance reasons, this will be Partial. However, after some period of idleness, it is generally assumed that the link will be inactive for an extended period of time and it is desirable to transition the link from Partial to Slumber. This can be done either by the host software or the device.

Since the host is best equipped to manage the PHY between commands and the best device within a command, the best power management is obtained when the host and device cooperate.

Link Power Management and Device State Interaction

The operating system can put devices into a D-state as defined by the Advanced Configuration and Power Interface (ACPI) specification [4]. Devices can include the host controller and the drive itself. The link, however, can be put into its power management state independent of the D-state of the host controller or the device.

Figure 9 illustrates the interaction between the link and the device D-states.

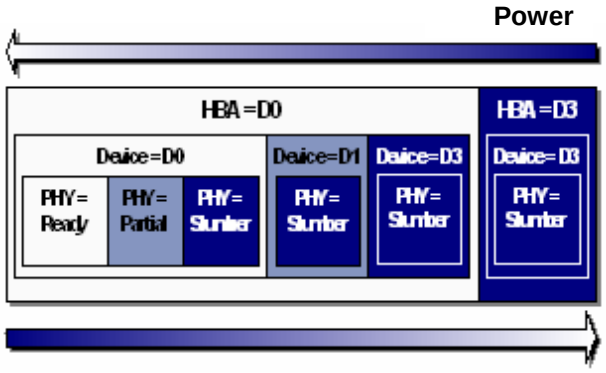

Figure 9: SATA Link and Device Power Management states

Here we see that all link power states are enabled when the device is in the D0 active state. When the device is in one of the lower power states, the link should be in Slumber.

Power Management Protocol and Results

The protocol for entering and exiting Partial and Slumber states is different. To enter one of the low-power states, the standard communication protocol between the host and device can be used. Once the PHY has been placed into a low-power state, the standard communication protocol between the host and drive cannot be used; another Out of Band (OOB) mechanism is required.

Entry Signaling Protocol

Either the host or the device can initiate a request to enter into the Partial or Slumber power state. The request is signaled by transmitting either the PMREQ_P or PMREQ_S primitive. PMREQ_P is used for a request to transition to the Partial power state, and PMREQ_S is used to transition to the Slumber power state. The

corresponding host or device must then respond with a PMACK acknowledge or PMNAK negative acknowledge primitive. If the request is acknowledged with a PMACK, both the host and device transition into the corresponding power state. To ensure the PMACK received is reliable without having to handshake the handshake, the target sends several PMACK's before entering a low-power state. If a PMNAK is received, no power state change occurs.

Exit Signaling Protocol

Once the PHY is in a low-power state, SATA specifies a low-level signaling mechanism to bring the interface back to active state. An OOB signal "COMWAKE" is sent to the device that acts as a wake-up call and causes communication to be reestablished.

Hardware/Software Control

Link Power Management is only enabled when the host controller and the device reports that it is capable of issuing or receiving requests, and the driver is capable of enabling the host hardware and drive. The host controller reports this capability to software in the Capabilities Register of the AHCI host controller (See [3] for details). The drive reports the ability to support these commands in the IDENTIFY_DEVICE data structure returned by the device during device enumeration (see the ATA [5] and SATAII [2] specifications for details). The host must specifically enable DIPM on the drive via the ATA SET_FEATURES command upon initialization.

Host/Device Design Recommendations and Interaction

The host hardware should transition the link into Partial after every command. Partial provides the best tradeoff between power savings and performance. The host should also transition the link into the Slumber state after requesting the drive to enter into a lower Advanced Configuration and Power Interface (ACPI) D-state.

In the absence of a host-initiated power management transition, the device should attempt to transition the link into Partial after some appropriate short timeout. Also, if the host doesn't transition the PHY into Slumber after sending a D-state command, the device should do it.

After a longer period of timeout, it can be assumed that the link will remain idle for a longer period of time. Either the host, through the host software, or the device should at this point transition the link to Slumber.

Device Removal During Power Management

SATA Link Power Management disables the PHY between the host and device. Because the PHY is disabled, a device removal cannot be immediately detected without waiting for the next command to be sent to the drive. The AHCI specification provides the capability for a second electrical signal to be provided to the host controller to notify the host that the drive has been removed. Typically this will be implemented as an interlock switch on the mobile platform.

Enabling Link Power Management in Software

SATA Link Power Management can be implemented in a variety of ways, two of which are presented here.

The first of these is the Intel Application Accelerator driver. The Intel Application Accelerator driver, supported on Windows operating systems, replaces the native Microsoft storage driver. It is provided with the ICH6-M chipset, and it utilizes the new AHCI interface. It implements the following AHCI-specific software features: Native Command Queuing, Native Hot Plug, Staggered Spinup, and Aggressive Link Power Management.

The Intel Application Accelerator driver unlocks the full potential of the new SATA bus through AHCI. It provides best-of-breed performance through Native Command Queuing, while reducing power consumption to a minimum through a full implementation of both host-initiated and device-initiated SATA Link Power management.

The second is through BIOS or other software cooperating with and using an existing legacy software stack. In this case the host controller is left in legacy mode, and no host-initiated link power management features, or other AHCI-related features, are available. In this case the BIOS or other software queries the drive through the ATA IDENTIFY_DEVICE data structure to determine its capability of supporting device-initiated link power management, and it enables it via the ATA SET_FEATURES command.

In BIOS this can be implemented using the _GTF ACPI object. For further details see the Advanced Configuration and Power Interface (ACPI) specification [4].

Power Measurement Results

In Figure 10 we show the chipset power consumption of an ICH6-M-based system at Windows idle. Here we see that a chipset with a hard disk on the SATA interface with Link Power Management active consumes nearly equivalent power to the chipset when connected to a PATA hard drive.

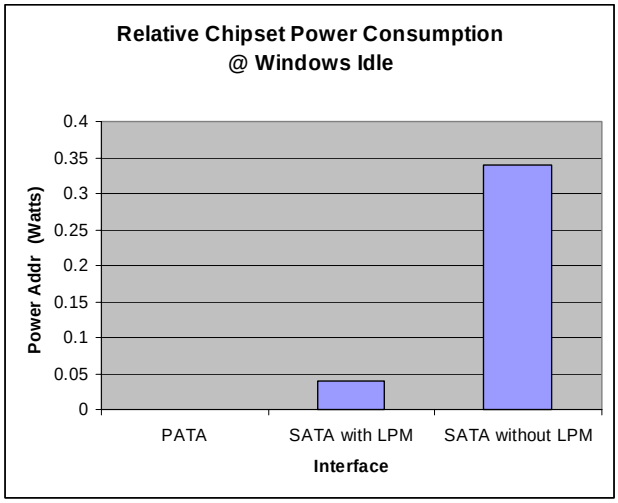

Figure 10: Power savings due to SATA link power management

Notice that Link Power Management provides nearly a 300 mW savings in the ICH6-M over a SATA drive without Link Power Management.

On the drive side, similar power savings can be achieved with a typical SATA hard disk drive consuming approximately 150 mW less power when Link Power Management is active. Total system-wide power savings attributable to Link Power Management in a single drive system reaches 450 mW.

INTEL HD AUDIO DISCUSSION

Intel HD Audio implementation in ICH6-M is the first instantiation of an Intel HD Audio host controller, along with the first generation of software. As the first instantiation, all of the features enabled by the Intel HD Audio architecture may not be available with a given codec or a given driver. Early instantiations have focused on higher quality audio (word size and bit rate), and have focused less on advanced features, such as array microphones and jack retasking.

Likewise, the power savings seen in a given instantiation of the platform will be very dependent on the codec and driver used. The power savings quoted in this paper were measured using an Intel mobile reference design.

The significance of the audio results is that Intel HD Audio provides meaningful increases in audio quality and functionality while reducing system power.

INTEL HD AUDIO CONCLUSION

Intel HD Audio provides significant improvement over prior integrated audio solutions. The ICH6-M implementation of the host controller supports improvements in audio quality and functionality. By carefully designing the architecture to minimize CPU interaction, Intel HD Audio was shown to save power relative to AC'97 in both DVD playback and CD playback. These savings were measured as 730 mW (DVD) and 850 mW (CD), which should result in prolonging battery life by 8 to 17 minutes for DVD playback, and by 35 to 42 minutes for CD playback. This shows that Intel HD Audio provides advanced capability while reducing system power.

SATA DISCUSSION

SATA Link Power Management was first implemented in the ICH6-M.

The Link Power Management results shown here were taken at Windows idle when no data were being transferred to the device. The system-level power savings realized by the end user will depend on the amount of disk traffic sent to the device. It is expected that with well-designed disk drives, and typical user loads, a typical user will experience nearly all of the 450 mW saved at Windows idle.

Furthermore, Link Power Management can be implemented on SATA optical drives as well as SATA hard drives. In typical mobile systems, the optical drive is rarely used. As the time of publication, SATA optical drives are not mature enough to measure the effect of Link Power Management, but by extrapolating from existing hard disk data we expect the optical drive to realize the same 150 mW savings that we see in the hard disk drive.

Total expected power savings in a typical 2 SATA drive system approach 600 mW, compared to a system without Link Power Management.

SATA CONCLUSIONS

SATA is an important technology to the Industry in that it provides a storage interconnect technology with room to grow over the next ten years. SATA provides significant improvements in storage performance and features for both desktop and mobile platforms. A significant challenge to the adoption of any new technology in the mobile space is power consumption. With a potential power savings of 600 mW, Link Power Management becomes an important component to the adoption rate of SATA in the mobile platform by providing the additional value of SATA with minimal power impact.

The Intel Application Accelerator driver provides the best implementation of Link Power Management, coupled with best-of-class performance through Native Command Queuing.

ACKNOWLEDGMENTS

Our thanks to Ed Pole and Les Cline for their valuable review feedback.

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AUTHORS' BIOGRAPHIES

Tom Clark is an I/O program manager for the Client Platform Division in Intel's Mobility Group. Tom is interested in integrating I/O technologies into core chipsets. He received his B.Sc. degree in Electrical Engineering from the University of Florida. His e-mail is thomas.m.clark at intel.com.

Feng (Frank) Yang is a software architect with the Mobility Group at Intel. He holds a Ph.D degree in Computer Science from Syracuse University. His current focus is on mobile platform technology. His e-mail is frank.yang at intel.com.

Greg Kaine received his B.S. degree in Computer Engineering from Purdue University at West Lafayette, IN and joined the Intel Rotation Engineering Program in 2001. Currently he is a platform architect in Intel's Mobility Group and is responsible for analysis of platform power and performance for mobile work loads. His current interests include analysis of mobile applications and multimedia workloads. His e-mail is greg.d.kaine at intel.com.

Brian Leete received his Bachelors degree in Electrical Engineering from Brigham Young University and is a software architect in Intel's Mobility Group, with background and interests in Serial Interconnect technologies, including SATA and USB, and driver- and OS-level software design and development. His e-mail is brian.a.leete at intel.com.

Sriram Ranganathan received his Bachelors degree in Mathematics in 1994, his Masters degree in Computer Application from Bharathidasan University in 1997, and his Masters degree in System Software from Birla Institute of Technology and Science in 1999. He works as a senior software engineer with Intel's Mobility Group. His current interest is in SATA and storage subsystems, and he has a background in developing system software and drivers for Windows and Linux* operating systems. His e-mail is sriram.ranganathan at intel.com.

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